CLEAN COPY OF ALL PENDING CLAIMS

- 1. A method of fabricating a semiconductor device comprising:
- (a) providing a semiconductor heterostructure comprising a relaxed Si_{1-x}Ge_x layer on a substrate, a strained channel layer on said relaxed Si_{1-x}Ge_x layer, and a Si_{1-y}Ge_y layer on said strained channel layer;
- (b) chemically reacting at least a portion of said Si_{1-y}Ge_y layer to form a chemically modified Si_{1-y}Ge_y layer on said strained channel layer;
- (c) removing said chemically modified Si_{1-y}Ge_y layer to expose said strained channel layer; and
 - (d) providing a dielectric layer on said exposed strained channel layer.

The method of claim 1 wherein step (b) comprises oxidizing said at least a portion of said Si_{1-y}Ge_y layer.

735. The method of claim 1 wherein said dielectric layer comprises a gate dielectric of a MISFET.

- 4. The method of claim 1 wherein the strained channel layer comprises Si.
- 5. The method of claim 1 wherein x is approximately equal to y.
- The method of claim II wherein step (a) further comprises providing a sacrificial Si layer on said Si_{1-y}Ge_y layer.
 - 7. 13. The method of claim 1 wherein y > x.
- 7. The method of claim 13 wherein step (a) further comprises providing a sacrificial Si layer on said Si_{1-y}Ge_y layer.
- The method of claim 14 wherein step (a) further comprises providing a sacrificial Si layer on said Si_{1-y}Ge_y layer having a thickness greater than the critical thickness.
- 16. The method of claim 1 wherein said substrate comprises Si.
- The method of claim 1 wherein said substrate comprises Si having a layer of SiO₂ thereon.





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The method of claim 1 wherein said substrate comprises a SiGe graded buffer layer on Si.

13.20. A method of fabricating a semiconductor device comprising:

- (a) providing a semiconductor heterostructure comprising a relaxed Si_{1-x}Ge_x layer on a substrate, a strained channel layer on said relaxed Si_{1-x}Ge_x layer, and a Si_{1-y}Ge_y layer on said strained channel layer;
 - (b) removing said Si_{1-y}Ge_y layer to expose said strained channel layer; and
 - (c) providing a dielectric layer on said exposed strained channel layer.

21. (Cancelled)

The method of claim 20 wherein step (c) comprises forming the gate dielectric of a MISFET by providing a dielectric layer on said exposed strained channel layer.

The method of claim 22 wherein step (c) comprises forming the gate dielectric of a MISFET by providing an oxide on said exposed strained channel layer.

The method of claim 20 wherein said strained channel comprises Si.

17:32. The method of claim 20 wherein said substrate comprises Si.

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32. The method of claim 20 wherein said substrate comprises Si having a layer of SiO₂ thereon.

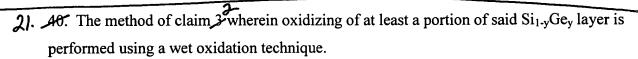
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34. The method of claim 20 wherein said substrate comprises a SiGe graded buffer layer on Si.

20:36. A method of fabricating a semiconductor device comprising the steps of:

(a) providing a semiconductor heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

- (b) removing said Si_{1-w}Ge_w layer to expose said Si layer; and
- (c) providing a dielectric layer on said Si layer.

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22'41. The method of claim 46 wherein said wet oxidation technique is utilized at a temperature up to about 750°C.

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42. The method of claim 20 wherein step (b) comprises removing said Si_{1-y}Ge_y layer to expose said strained channel layer using either wet or dry etch technique.

The method of claim 20 further comprising the step of removing at least a portion of the strained channel layer to eliminate residual Ge.

25.4. The method of claim 36 wherein step (b) comprises removing said Si_{1-w}Ge_w layer to expose said Si layer using either wet or dry etch technique.

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